AMENDMENTS TO THE CLAIMS:

1-30 (Cancelled)

31. (Currently Amended) A semiconductor package comprising:

a die pad having opposed, generally planar first and second surfaces, and peripheral side surfaces which extend between the first and second surfaces;

a plurality of leads extending at least partially about the die pad in spaced relation to the side surfaces thereof, each of the leads having:

opposed, generally planar first and second surfaces;

peripheral side surfaces extending between the first and second surfaces;

an inner lead portion defining an inner end surface; and

an outer lead portion, a portion of the first surface defined by the outer lead portion being sized and configured for electrical connection to a conductive terminal;

a semiconductor chip **including an active surface having a plurality of conductive bond pads thereon, a portion of the active surface being** attached to the first surface of the die pad**, with the semiconductor chip and the leads being sized and oriented relative to each other such that each of the bond pads at least partially overlaps** and **is** electrically connected to ~~**at least**~~ **the first surface of a respective** one of the leads; and

a package body at least partially encapsulating the semiconductor chip, the die pad, and the leads such that the inner lead portion of each of the leads is within the package body and the outer lead portion of each of the leads extends out of the package body.

32. (Original) The semiconductor package of Claim 31 wherein the inner end surface of each of the leads and portions of the first and side surfaces of each of the leads which extend along the inner lead portion thereof are covered by the package body.

33. (Original) The semiconductor package of Claim 32 wherein:

the package body has opposed, generally planar first and second surfaces; and

a portion of the second surface of each of the leads which extends along the inner lead portion thereof is exposed in and substantially flush with the second surface of the package body.

34. (Previously Presented) The semiconductor package of Claim 33 wherein the first and side surfaces of the die pad are covered by the package body.

35. (Previously Presented) The semiconductor package of Claim 34 wherein the second surface of the die pad is exposed in and substantially flush with the second surface of the package body.

36. (Cancelled)

37. (Cancelled)

38. (Original) The semiconductor package of Claim 31 wherein:

each of the leads includes an undercut region which is disposed in the second surface thereof and extends to the inner end surface thereof; and

the undercut region of each of the leads is covered by the package body.

39. (Original) The semiconductor package of Claim 38 wherein:

the die pad includes an undercut region which is disposed in the second surface thereof and extends to the side surfaces thereof; and

the undercut region of the die pad is covered by the package body.

40. (Original) The semiconductor package of Claim 31 further in combination with a second semiconductor chip attached to the semiconductor chip and electrically connected to at least one of the leads, the second semiconductor chip being covered by the package body.

41. (Original) A semiconductor package comprising:

a die pad having opposed, generally planar first and second surfaces, and peripheral side surfaces which extend between the first and second surfaces;

a plurality of leads extending at least partially about the die pad in spaced relation to the side surfaces thereof, each of the leads having:

opposed, generally planar first and second surfaces;

peripheral side surfaces extending between the first and second surfaces;

an inner lead portion defining an inner end surface; and

an outer lead portion;

a package body at least partially encapsulating the die pad and the leads such that the first surface of the die pad and a portion of the first surface of each of the leads extending along the inner lead portion thereof are exposed in a cavity defined by the package body, and the outer lead portion of each of the leads extends out of the package body; and

a semiconductor chip disposed within the cavity and attached to the first surface of the die pad, the semiconductor chip being electrically connected to at least one of the leads.

42. (Original) The semiconductor package of Claim 41 wherein the inner end surface of each of the leads and portions of the side surfaces of each of the leads which extend along the inner lead portion thereof are covered by the package body.

43. (Original) The semiconductor package of Claim 42 wherein:

the package body has a generally planar second surface; and

a portion of the second surface of each of the leads which extends along the inner lead portion thereof is exposed in and substantially flush with the second surface of the package body.

44. (Previously Presented) The semiconductor package of Claim 43 wherein the first and side surfaces of the die pad are covered by the package body.

45. (Previously Presented) The semiconductor package of Claim 44 wherein the second surface of the die pad is exposed in and substantially flush with the second surface of the package body.

46. (Original) The semiconductor package of Claim 41 wherein the semiconductor chip is electrically connected to the first surface of at least one of the leads via a conductive wire which is disposed within the cavity of the package body.

47. (Currently Amended) The semiconductor package of Claim ~~31~~ 41 further in combination with a lid attached to the package body and enclosing the cavity thereof.

48. (Cancelled)

49. (Cancelled)

50. (Cancelled)